FPGA CONFIGURATION MEMORY WITH BUILT-IN ERROR CORRECTION MECHANISM

ABSTRACT

A system and method are disclosed for error correction in a programmable logic device (PLD). A frame circuit retrieves data from each column of configuration memory of the PLD, and a check memory stores of a plurality of check words. A buffer circuit is coupled to the check memory and to the frame circuit. The buffer circuit assembles blocks of data from data retrieved by the frame circuit and from corresponding check words in the check memory. A plurality of storage elements are provided for storage of status information. A check circuit is coupled to the storage elements and to the buffer circuit. Each block is checked by the check circuit using an error correcting code, and data indicating detected errors is stored in the storage elements.